

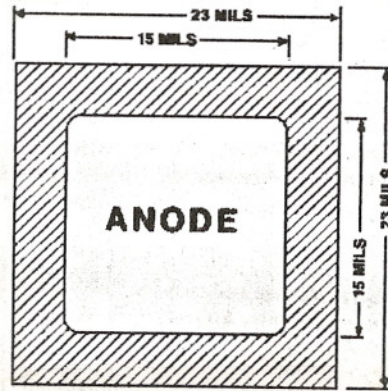


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: Al**  
**Backside: Au**  
**Backside Potential: Cathode**  
**Mask Ref: Issue 1**  
**Bond Pads: see above**

**APPROVED BY: CD**

**MFG: CDI**

**DIE SIZE: .023" x .023"**

**THICKNESS: .010" +/- .002"**

**DATE: 7/25/02**

**P/N: GI1440**